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10/587,845	07/28/2006	Risho Koh	040373-0396	9910

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EXAMINER	
TRAN, TRANG Q	
ART UNIT	PAPER NUMBER
2811	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,845	KOH ET AL.	
	Examiner	Art Unit	
	TRANG Q. TRAN	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-89* is/are pending in the application.

4a) Of the above claim(s) *12-32,48 and 53-89* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,33-47 and 49-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/28/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species I (Fig. 1, claim 1-11 and 33-52) in the reply filed on October 27, 2008 is acknowledged.

Claims 12-32 and 53-89 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on October 27, 2008.

Claim 49 is withdrawn from further consideration because claim 49 comprises a cap insulating layer which below to Embodiment of Fig. 44 A and 44B.

Claim Objections

Claim 1 and 2 is objected to because of the following informalities:

The recited limitation of "the lower part of the semiconductor layer" of claim 1 is unclear. Appropriate correction is required.

The recited limitation of "the upper part of the semiconductor layer" of claim 1 is unclear. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 and 33-48, and 50-52 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re. claim 1, the recited limitation of "opposite side surfaces" is unclear as to which side surface the applicant refers. How can be a gate provided on opposite side surfaces?

The recited limitation of "the side surface" is unclear as to which side surface the applicant refers.

Re, claims 1 and 2, the limitation of "wherein said semiconductor layer has a channel forming region in a portion sandwiched between said source/drain regions, and has on the upper part of the semiconductor layer in the channel forming region a channel impurity concentration adjusting region of which the concentration of a second conductivity type impurity is higher than that of the lower part of the semiconductor layer", as recited in claims 1 and 2 is unclear as to which has on the upper part of the semiconductor layer and which layer has second conductivity type impurity that the applicant refers. What does "that" refer to? Does the first and second conductivity have the same conductive type?

The limitation of "in the channel impurity concentration adjusting region, a channel is formed on a side surface portion of the semiconductor layer in the channel impurity concentration adjusting region", as recited in claims 1 and 2, is unclear.

Re. claim 2, the recited limitation of "a gate electrode.....to facing opposite side surfaces" is unclear. How can be a single gate face opposite side surfaces?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Inaba et al. (US 2002/0036290).

Re. claim 1, Fig. 7 of Inaba discloses a field effect transistor comprising:

a semiconductor layer (11) projecting upward from the plane of a base (as seen in Fig. 7);

a gate electrode (14) provided on opposite side surfaces of the semiconductor layer (1);

a gate insulating film (13) interposed between the gate electrode (14) and the side surface of said semiconductor layer (11); and

source/drain regions (15+16) where a first conductivity type impurity (N-type) is introduced in said semiconductor layer (as seen in Fig. 7),

wherein said semiconductor layer (11) has a channel forming region in a portion sandwiched between said source/drain regions (as seen in Fig. 7), and has on the upper part of the semiconductor layer in the channel forming region a channel impurity concentration adjusting region (21) of which the concentration of a second conductivity

type impurity (P+) is higher than that of the lower part of the semiconductor layer (11), and

in the channel impurity concentration adjusting region, a channel (11A) is formed on a side surface portion of the semiconductor layer (11) in the channel impurity concentration adjusting region (21), which faces said gate insulating film (13), "in a state of operation in which a signal voltage is applied to said gate electrode" (see note 1 below).

Re. claim 2, Fig. 7 of Inaba discloses a field effect transistor comprising:

a semiconductor layer (11) projecting upward from the plane of a base (as seen in Fig. 7);

a gate electrode (14) extending from the upper part of the semiconductor layer to facing opposite side surfaces so as to straddle the semiconductor layer (as seen in Fig. 7);

a gate insulating film (13) interposed between the gate electrode (14) and said semiconductor layer (11); and

source/drain regions (15+16) where a first conductivity type impurity (N) is introduced in said semiconductor layer (11),

wherein said semiconductor layer (11) has a channel forming region in a portion sandwiched between said source/drain regions (as seen in Fig. 7), and has on the upper part of the semiconductor layer in the channel forming region a channel impurity concentration adjusting region (21) of which the concentration of a second conductivity

type impurity (P+) is higher than that of the lower part of the semiconductor layer (11), and

in the channel impurity concentration adjusting region, a channel (11A) is formed on a side surface portion of the semiconductor layer (11) in the channel impurity concentration adjusting region (21), which faces said gate insulating film (13), "in a state of operation in which a signal voltage is applied to said gate electrode" (see note 1 below).

Re. claim 3, Inaba discloses the field effect transistor according to claim 1, wherein when having in the upper part of the semiconductor layer (11) a concentration of the second conductivity type impurity (P-type) which is same as that in the lower part of the semiconductor layer (as seen in Fig. 7), said channel impurity concentration adjusting region (21) has an impurity concentration (P+) with "which an electric potential increasing in a corner portion of the upper part of the semiconductor layer can be reduced for an n-channel transistor; and a reduction in electric potential in the corner portion of the upper part of the semiconductor layer can be downscaled for a p-channel transistor" (see note 2 below).

Re. claim 4, Inaba discloses the field effect transistor according to claim 1, wherein said channel impurity concentration adjusting region (21) has an impurity concentration (P+) with "which an electric potential increasing in the corner portion of the upper part of the semiconductor layer can be reduced by 60 mV or more for the n-

channel transistor; and a reduction in electric potential in the corner portion of the upper part of the semiconductor layer can be downscaled by 60 mV or more for the p-channel transistor" (See note 2 below).

Re. claim 52, Inaba discloses the field effect transistor according to claim 1, wherein in said channel forming region excepting said channel impurity concentration adjusting region, "an electric potential on the side surface of the semiconductor layer increases by 120 mV or more for the n-channel transistor and decreases by 120 mV or more for the p-channel transistor with respect to an electric potential at the central portion of the semiconductor layer" (See Note 2).

Note 1: The recited limitation is drawn to a process by which the product is made. Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. Because the product by process does not change the end product, Applicant's claimed invention does not distinguish over prior art. See MPEP § 2113.

Note 2: A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is

capable of performing the intended use, then it meets the claim. In essence, apparatus claims cover what a device is, not what a device does. See MPEP § 2112.01 and § 2114.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-11 and 33-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba.

Re. claim 5, Inaba discloses the field effect transistor according to claim 1, Inaba further teaches the other region (11) below the channel has concentration of the second conductivity type impurity (P-type) and concentration of the second conductivity type impurity (P+) in said channel impurity concentration adjusting region (7). However, Inaba may not explicitly teach wherein the average value of the net concentration of the second conductivity type impurity in said channel impurity concentration adjusting region is in a range from 1.3 times or more to 4 times or less as large as the average value of the net concentration of the second conductivity type impurity in other regions below the channel impurity concentration adjusting region.

It would have been obvious to one of ordinary skill in the art the time the invention was made to provide claimed average value of net concentration of Inaba in order to achieve the device properties.

Since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranged involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Re. claims 6, 10, 36-39 and 48 Same reason as claim 5 rejection

Re. claim 7, Inaba discloses the field effect transistor according to claim 1, Inaba teach the channel impurity concentration adjusting region has a certain depth and with. Inaba may not explicitly teach wherein in said channel impurity concentration adjusting region, a depth Htop extending downward from the upper end of said semiconductor layer is 0.7 (or 7/40) times or less as large as a width Wfin of the semiconductor layer parallel to the plane of the base and vertical to the longitudinal direction of the channel.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide claimed measurement such as depth and thickness, since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233; *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996).

Re. claims 8-9, and 40-45, Same reason as claim 7 rejection.

Re. claim 11, Inaba discloses the field effect transistor according to claim 1, wherein said channel impurity concentration adjusting region (21) is provided along an entire in-plane direction parallel to the plane of the base in the upper part of the semiconductor layer (11) in said channel forming region (as seen in Fig. 7).

Re. claim 33, Inaba discloses the field effect transistor according to claim 1, wherein said semiconductor layer has an upper channel impurity concentration adjusting region (21) which is said channel impurity concentration adjusting region (21) provided in the upper part of the semiconductor layer (11), a middle channel forming region (middle portion of the channel which forms in 11A) which is provided below the upper channel impurity concentration adjusting region (21) and of which the concentration of the second conductivity type impurity (P) is lower than that in the upper channel impurity (P+) concentration adjusting region, and a lower channel impurity concentration adjusting region (lower portion of the channel which form in 11A) which is provided in the lower part of the semiconductor layer below the middle channel forming region.

Inaba may not explicitly teach the concentration of the second conductivity type impurity is higher than that in the middle channel forming region.

It would have been obvious to one of ordinary skill in the art the time the invention was made to provide the concentration of the second conductivity type

impurity is higher than that in the middle channel forming region of Inaba in order to achieve the device properties.

Since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranged involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Re. claim 34, Inaba discloses the field effect transistor according to claim 33, wherein said lower channel impurity concentration adjusting region (lower portion of the channel) has a channel formed in a side surface portion of the semiconductor layer (11) in the lower channel impurity concentration adjusting region, which faces said gate insulating film (13), "in a state of operation in which a signal voltage is applied to said gate electrode" (See Note 1).

Re. claim 35, Inaba discloses the field effect transistor according to claim 33, wherein said lower channel impurity concentration adjusting region (lower portion of the channel) has an impurity concentration (P) with "which an electric potential increasing in the corner portion of the lower part of the semiconductor layer can be reduced (See Note 2) when said lower channel impurity concentration adjusting region (lower portion of the channel) has a concentration of the second conductivity type impurity (P) which is same as that in said middle channel forming region (middle portion of the channel).

Re. claim 46, Inaba discloses the field effect transistor according to claim 33, wherein said lower channel impurity concentration adjusting region (lower portion of the channel) is provided along an entire in-plane direction parallel to the plane of the base in the lower part of the semiconductor layer (11) in the portion sandwiched between source/drain regions (15+16) (as seen in Fig. 7).

Re. claim 47, Inaba discloses the field effect transistor according to claim 33, wherein the field effect transistor has as said lower channel impurity concentration adjusting region (lower portion of the channel) the channel impurity concentration adjusting region so as to include at least a part of the corner portion of the semiconductor layer (11) in the lower part of the semiconductor layer in the portion sandwiched between said source/drain regions (15+16), and further has a portion which does not have the lower channel impurity concentration adjusting region in a section parallel to the plane of the base, which includes the lower channel impurity concentration adjusting region (as seen in Fig. 7).

Re. claim 49, Inaba discloses the field effect transistor according to claim 1, wherein a cap insulating film (12) thicker than said gate insulating film (13) is provided between the upper part of said semiconductor layer (11) and said gate electrode (14) so that no channel is formed on the upper surface of the semiconductor layer (as seen in Fig, 7).

Re. claim 50, Inaba discloses the field effect transistor according to claim 1, wherein the field effect transistor has a support substrate under said projecting semiconductor layer (11A), and the semiconductor layer is connected integrally to the support substrate (as seen in Fig. 7).

Re. claim 51, Inaba discloses the field effect transistor according to claim 1, wherein the field effect transistor has a support substrate (11) under said projecting semiconductor layer (11A), and the semiconductor layer (11) is provided on the support substrate via a buried insulating film (12).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRANG Q. TRAN whose telephone number is (571)270-3259. The examiner can normally be reached on Mon - Thu (9am-5pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. Q. T./
Examiner, Art Unit 2811
/Cuong Q Nguyen/
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